[10901/81]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Roman WOYZICHOVSKI
Serial No.:	10/501,310
Filed:	November 23, 2004
For:	METHOD FOR INTERPOLATING AT LEAST TWO POSITION-DEPENDENT, PERIODIC ANALOG SIGNALS THAT ARE DEPHASED RELATIVE TO EACH OTHER
Examiner:	Jason Perilla
Art Unit:	2611
Confirmation No.	6114

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Signature:/Julie Forero/

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

SIR:

On January 29, 2009, Appellant filed a Notice of Appeal from the last decision of the Examiner contained in the Final Office Action dated September 5, 2008 in the above-identified patent application.

In accordance with 37 C.F.R. § 41.37, this brief is submitted in support of the appeal of the rejections of claims 21 to 42. For at least the reasons set forth below, the rejections of claims 21 to 42 should be reversed.

1. REAL PARTY IN INTEREST

The real party in interest in the present appeal is DR. JOHANNES HEIDENHAIN GmbH of Traunreut, Federal Republic of Germany, which is the assignee of the entire right, title and interest in and to the present application.

2. RELATED APPEALS AND INTERFERENCES

There are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellant or the assignee, DR. JOHANNES HEIDENHAIN GmbH, "which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal."

3. STATUS OF CLAIMS

Claims 1 to 20 have been canceled.

Claims 21 to 42 are pending.

Claims 21 to 24, 26, 27, and 30 to 42[1] stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of U.S. Patent No. 5,079,549 ("Liessner") and U.S. Patent No. 5,134,578 ("Garverick et al.").

Claim 25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Liessner, Garverick et al., and that which the Final Office Action considers to constitute admitted prior art ("the AAPA").

Claims 28 and 29 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Liessner, Garverick et al., and U.S. Patent Application Publication No. 2002/0116181 ("Khan et al.").

A copy of the appealed claims, *i.e.*, claims 21 to 42, is attached hereto in the Claims Appendix.

4. STATUS OF AMENDMENTS

In response to the Final Office Action dated September 5, 2008, Appellant filed a "Reply Under 37 C.F.R. § 1.116" ("the Reply") on December 4, 2008. The Reply presented proposed amendments to claim 29 to address a rejection raised in the Final Office

[1]The Final Office Action states on page 5 that "[c]laims 21-24, 26, 27, and 30-***40*** are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner . . . in view of Garverick et al." (emphasis added). However, page 10 of the Final Office Action suggests that claims 41 and 42 were intended to be included among the claims rejected on this ground. Thus, Appellant addresses this rejection in this Appeal Brief as though claims 41 and 42 were rejected under 35 U.S.C. § 103(a) based on Liessner and Garverick et al.

Action under 35 U.S.C. § 112, second paragraph. The Advisory Action dated December 22, 2008 states that the proposed amendments will be entered for the purposes of appeal (and indicates that the rejection raised under 35 U.S.C. § 112, second paragraph will be withdrawn for the purposes of appeal). It is therefore Appellant's understanding that the claims as included in the annexed "Claims Appendix" reflect the current claims.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present claims on appeal include four independent claims, *i.e.*, claims 21, 40, 41, and 42.

Independent claim 21 relates to a method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale. Claim 21 recites that the method includes converting each of the analog signals *a1*, *a2* into a digital data stream *s1*, *s2* by a sigma-delta modulator *3*. *Specification*, page 6, lines 28 to 29 and page 8, lines 2 to 16; Figure 1. Claim 21 recites that the method includes generating a string of results *d* by combining the data streams *s1*, *s2* with correctional values *k1*, *k2* and subsequently combining the data streams *s1*, *s2* with one another. *Specification*, page 6, lines 30 to 32 and page 10, lines 9 to 18; Figure 1. Claim 21 recites that method includes generating from the string of results *d* (a) new correctional values *k1*, *k2* in accordance with a quality criterion *k3* that is to be satisfied during interpolation and (b) output signals *w* of the interpolation. *Specification*, page 6, lines 32 to 35 and page 8, line 28 to page 9, line 1; Figure 1. Claim 21 recites that the method includes accumulating over a specifiable time interval values of the string of results *d* for generating the correctional values *k1*, *k2* and the output signals *w*. *Specification*, page 6, lines 35 to 37; Figure 1. Claim 21 recites that the method includes using a signal sequence *a* generated by the accumulation as an address sequence for generating the correctional values *k1*, *k2* and for generating the output signal *w*. *Specification*, page 7, lines 1 to 3 and page 10, lines 20 to 29; Figure 1.

Independent claim 40 relates to a device for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to each other and which are generated by scanning a measuring scale. Claim 40 recites that the device includes a sigma-delta modulator *3* configured to convert the analog signals *a1*, *a2* to a respective digital data stream *s1*, *s2*. *Specification*, page 7, lines 9 to 10 and page 8, lines 2 to 16; Figure 1. Claim 40 recites that the device includes an arithmetic unit *5* configured to generate a string of results *d* in accordance with a combination of the data streams *s1*, *s2* with

correctional values *k1*, *k2* and in accordance with subsequent combination of the data streams *s1*, *s2* with one another. *Specification*, page 7, lines 10 to 14 and page 10, lines 9 to 18; Figure 1. Claim 40 recites that the device includes an arrangement configured to generate, from the string of results *d*, (a) new correctional values *k1*, *k2* in accordance with a quality criterion *k3* that is to be satisfied during the interpolation and (b) output signals *w* of the interpolation. *Specification*, page 7, lines 14 to 18 and 32 to 35 and page 8, line 28 to page 9, line 1; Figure 1. Claim 40 recites that the device includes a filter *9* configured to accumulate values of the string of results *d* over a specified time interval to generate an address sequence *a* to control the arithmetic unit *5* to guide the string of results *d* to satisfy the quality criterion *k3*. *Specification*, page 7, lines 18 to 22; Figure 1. Claim 40 recites that the device includes an evaluation circuit *10* post-connected to the filter *9* configured to convert address values of the address sequence *a* into output values *w* of the interpolation. *Specification*, page 7, lines 22 to 25.

Independent claim 41 relates to a method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale. Claim 41 recites that the method includes converting each of the analog signals *a1*, *a2* into a digital data stream *s1*, *s2* by a sigma-delta modulator *3*. *Specification*, page 6, lines 28 to 29 and page 8, lines 2 to 16; Figure 1. Claim 41 recites that the method includes generating a string of results *d* by combining the data streams *s1*, *s2* with correctional values *k1*, *k2* and subsequently combining the data streams *s1*, *s2* with one another. *Specification*, page 6, lines 30 to 32 and page 10, lines 9 to 18; Figure 1. Claim 41 recites that the method includes generating from the string of results *d* a combination output in accordance with a quality criterion *k3* that is to be satisfied during interpolation. *Specification*, page 8, lines 28 to 32; Figure 1. Claim 41 recites that the method includes accumulating over a specifiable time interval values of the combination output for generating the correctional values *k1*, *k2* and output signals *w*. *Specification*, page 8, lines 28 to 32; Figure 1. Claim 41 recites that the method includes using a signal sequence *a* generated by the accumulation as an address sequence for generating the correctional values *k1*, *k2* and for generating the output signal *w*. *Specification*, page 7, lines 1 to 3 and page 10, lines 20 to 29; Figure 1.

Independent claim 42 relates to a device for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to each other and which are generated by scanning a measuring scale. Claim 42 recites that the device includes a sigma-delta modulator *3* configured to convert the analog signals *a1*, *a2* to a respective

digital data stream *s1*, *s2*. *Specification*, page 7, lines 9 to 10 and page 8, lines 2 to 16; Figure 1. Claim 42 recites that the device includes an arithmetic unit *5* configured to generate a string of results *d* in accordance with a combination of the data streams *s1*, *s2* with correctional values *k1*, *k2* and subsequent combination of the data streams *s1*, *s2* with one another. *Specification*, page 7, lines 10 to 14 and page 10, lines 9 to 18; Figure 1. Claim 42 recites that the device includes an arrangement configured to generate, from the string of results *d* a combination output in accordance with a quality criterion *k3* that is to be satisfied during the interpolation. *Specification*, page 8, lines 28 to 32; Figure 1. Claim 42 recites that the device includes a filter *9* configured to accumulate values of the combination output over a specified time interval to generate an address sequence *a* to control the arithmetic unit *5* to guide the string of results *d* to satisfy the quality criterion *k3*. *Specification*, page 7, lines 18 to 20; Figure 1. Claim 42 recites that the device includes an evaluation circuit *10* post-connected to the filter *9* configured to convert address values of the address sequence *a* into output values *w* of the interpolation. *Specification*, page 7, lines 22 to 25; Figure 1.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 21 to 24, 26, 27, and 30 to 42 are unpatentable, under 35 U.S.C. § 103(a), over the combination of Liessner and Garverick et al.

B. Whether claim 25 is unpatentable, under 35 U.S.C. § 103(a), over the combination of Liessner, Garverick et al., and the AAPA.

C. Whether claims 28 and 29 are unpatentable, under 35 U.S.C. § 103(a), over the combination of Liessner, Garverick et al., and Khan et al. Whether claims 1 to 14 are anticipated, under 35 U.S.C. § 102(e), by Nelson et al.

7. ARGUMENTS

A. Rejection of Claims 21 to 24, 26, 27, and 30 to 42 Under 35 U.S.C. § 103(a)

Claims 21 to 24, 26, 27, and 30 to 42 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Liessner and Garverick et al. For at least the reasons more fully set forth below, it is respectfully submitted that the present rejection should be reversed.

Claim 21, for example, relates to a method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale. According to claim 21, the method includes converting each of the analog signals into a digital data stream by a sigma-delta

modulator. By combining the data streams with correctional values and subsequently combining the data streams with one another, a string of results is generated. The method further includes generating from the string of results (a) new correctional values in accordance with a quality criterion that is to be satisfied during interpolation and (b) output signals of the interpolation. Over a specifiable time interval, values of the string of results are accumulated for generating the correctional values and the output signals. A signal sequence generated by the accumulation is thus used as an address sequence for generating the correctional values and for generating the output signal.

In contrast to the foregoing, the entire functionality and structure described by Liessner is ***analog*** and not in any manner ***digital***. In this regard, Liessner describes that the input signal to the system is an ***analog*** representation of a displacement and that an encoder 10 provides ***analog*** signals to multipliers 12, 14. Col. 3, lines 15 to 21. Liessner further describes that each multiplier 12, 14 provides an ***analog*** signal to adder 20. Col. 3, lines 41 to 44. Thus, there is no disclosure, or even any suggestion, by Liessner of converting ***analog*** signals, which are generated by scanning a measuring scale, into a ***digital*** data stream by a sigma-delta modulator or otherwise. Furthermore, the only conversion described by Liessner between analog and digital signals is in connection with multipliers 12, 14, which are described by Liessner as being ***digital-to-analog*** (not ***analog-to-digital***) converters that cause a ***digital input*** to attenuate an analog current reference signal. Thus, Liessner in no manner describes, or even suggests, an ***analog-to-digital*** conversion. Indeed, even the output signal ES is described by Liessner as being an ***analog*** error signal. Col. 3, lines 43 to 44. There is no discussion whatsoever by Liessner of whether, how or even why any of the ***analog*** devices might be modified to ***digital*** devices or whether or how ***digital*** data streams might be handled.

Moreover, Appellant respectfully submits that the proposed modification would change the entire principle of operation of the resolver described by Liessner, *e.g.*, the modification would require substantial reconstruction and redesign of the components described by Liessner as well as a change in the basic principle under which the device described by Liessner is designed to operate. As such, the proposed modification is insufficient to render obvious the present claims. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959) (if the proposed modification would change the principle of operation of a prior art device being modified, then the references are *insufficient* to render the claims *prima facie* obvious). The mere reference to sigma-delta analog to digital converters in Garverick et al. does not in any manner cure the critical deficiencies set forth above.

Furthermore, Liessner does not disclose, or even suggest, accumulating, over a specifiable time interval, values of strings of results for generating correction values and output signals. As described, for example, in col. 3, line 41 to col. 4, line 64 and with reference to Figure 6, generation of counting signals is only based on the value of the analog error signal ES and ***not*** in any manner upon a time interval. In this regard, the following possibilities exist according to Liessner: (1) if the value of the error signal ES is inside of the dead zone, i.e., between +REF.1 and -REF.1, no counting occurs; (2) if the value of the error signal ES is between +REF.1 and +REF.2 or between -REF.1 and -REF.2, i.e., within the single step zone, slow count pulses are generated; and (3) if the value of the error signal ES is greater than +REF.2 or lower than -REF.2, *i.e.*, in the multi-step zone, fast count pulses are generated. However, a change from one zone to another only depends upon the value of the analog error signal. That there is no disclosure by Liessner of accumulation, over a specifiable time interval, the Board's attention is respectfully directed to, *e.g.*, col. 4, lines 39 to 43, which state that "the asynchronous count generator 24 operates ***without employing a clock signal***" and that "the circuitry of generator 24 responds promptly to an incoming signal from an output of the detector 22." In this regard, the Board's attention is also respectfully directed to col. 1, lines 51 to 68 of Liessner, which describes "***critical limitations***" associated with employing a clock signal in the overall performance of an interpolator. The foregoing makes perfectly clear that Liessner does not disclose, or even suggest, accumulating, over a specifiable time interval, values of a string of results for generating correction values and output signals as recited in claim 21. Liessner does not disclose, or even suggest, the accumulating recited in claim 41 or the filter recited in claims 40 and 42 for analogous reasons. In addition to Liessner's failure to disclose, or even suggest, accumulating as recited in claims 21 and 41 and a filter as recited in claims 40 and 42, Liessner ***teaches away from*** employing a clock signal, as mentioned at col. 1, lines 51 to 68 and col. 4, lines 39 to 43.

Based on the foregoing, it is plainly apparent that the combination of Liessner and Garverick et al. does not disclose, or even suggest, all of the features included in claims 21 and 40 to 42. As such, the combination of Liessner and Garverick et al. does not render unpatentable claims 21 and 40 to 42.

While the Final Office Action contends that "[o]ne skilled in the art would be . . . motivated to complete the conversion because of the advantages provided by digital implementations of analog devices," the Final Office Action plainly fails to adequately set forth a *prima facie* case of obviousness based upon a motivation-to-combine rationale consistent with the Supreme Court's *KSR* decision (*KSR International Co. v. Teleflex Inc.*, 82

U.S.P.Q.2d 1385 (2007)) or the guidelines set forth in M.P.E.P. § 2141. As stated in M.P.E.P. § 2141, to reject a claim based on a motivation-to-combine rationale, Office personnel ***must*** resolve the factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459 (1966) ***and then*** articulate: (1) a finding that there was some teaching, suggestion, or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings; (2) a finding that there was a reasonable expectation of success; ***and*** (3) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness. The Final Office Action has completely failed in this regard. Accordingly, a *prima facie* case of obviousness has not been adequately set forth in the Office Action.

In addition, the present rejection fails to consider either Liessner or Garverick et al. in its entirety, *i.e.*, as a *whole*, including those portions that teach away from the claimed subject matter, as required for a proper analysis under 35 U.S.C. § 103(a). *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). As indicated above, Liessner specifically criticizes, discredits, and discourages employing a clock signal and thus teaches away from the claimed subject matter, including: accumulating ***over a specifiable time interval*** values of a string of results for generating correction values and an output signal, in the context of claim 21; a filter configured to accumulate values of a string of results over a ***specified time interval*** to generate an address sequence to control an arithmetic unit to guide a string of results to satisfy a quality criterion, in the context of claim 40; accumulating ***over a specifiable time interval*** values of a combination output for generating correction values and output signals, in the context of claim 41; and a filter configured to accumulate values of a combination output over a ***specified time interval*** to generate an address sequence to control an arithmetic unit to guide a string of results to satisfy a quality criterion, in the context of claim 42. Without a clock signal, the foregoing features cannot be present. Since Liessner specifically teaches away from the claimed subject matter, it is respectfully submitted that an obviousness rejection of the present claims based on Liessner cannot be sustained.

In view of all of the foregoing, it is respectfully submitted that the combination of Liessner and Garverick et al. does not render unpatentable claims 21, and 40 to 42.

As for claims 22 to 24, 26, 27 and 30 to 39, which ultimately depend from claim 21 and therefore include all of the features included in claim 21, it is respectfully

submitted that the combination of Liessner and Garverick et al. does not render unpatentable these dependent claims for at least the reasons more fully set forth above in support of the patentability of claim 21.

In view of all of the foregoing, reversal of this rejection is respectfully requested.

B. Rejection of Claim 25 Under 35 U.S.C. § 103(a)

Claim 25 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Liessner, Garverick et al., and AAPA For at least the reasons more fully set forth below, it is respectfully submitted that the present rejection should be reversed.

As an initial matter, Appellant does not necessarily agree with the contention that the Specification contains an admission that "low-pass filtering and assignment of the address values is well known in the art." Notwithstanding the foregoing, it is respectfully submitted that the combination of Liessner, Garverick et al., and the AAPA does not render unpatentable claim 25 for the following additional reasons.

Claim 25 ultimately depends from claim 21 and therefore includes all of the features included in claim 21. As more fully set forth above, the combination of Liessner and Garverick et al. does not render unpatentable claim 21, from which claim 25 ultimately depends. The AAPA does not cure the critical deficiencies of the combination of Liessner and Garverick et al. As such, the combination of Liessner, Garverick et al., and the AAPA does not render unpatentable claim 25, which ultimately depends from claim 21. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988) (any dependent claim that depends from a non-obvious independent claim is non-obvious).

In view of all of the foregoing, reversal of this rejection is respectfully requested.

C. Rejection of Claims 28 and 29 Under 35 U.S.C. § 103(a)

Claims 28 and 29 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Liessner, Garverick et al., and Khan et al. For at least the reasons more fully set forth below, it is respectfully submitted that the present rejection should be reversed.

Claims 28 and 29 ultimately depend from claim 21 and therefore include all of the features included in claim 21. As more fully set forth above, the combination of Liessner and Garverick et al. does not render unpatentable claim 21, from which claims 28 and 29 ultimately depend. Khan et al. does not cure the critical deficiencies of the combination of

Liessner and Garverick et al. As such, the combination of Liessner, Garverick et al., and Khan et al. does not render unpatentable claims 28 and 29, which ultimately depend from claim 21. *Id.*

In view of all of the foregoing, reversal of this rejection is respectfully requested.

8. CLAIMS APPENDIX

A "Claims Appendix" is attached hereto and appears on the four (4) pages numbered "Claims Appendix 1" to "Claims Appendix 4."

9. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellant in the appeal. An "Evidence Appendix" is nevertheless attached hereto and appears on the one (1) page numbered "Evidence Appendix."

10. RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2, above, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellant or the assignee, DR. JOHANNES HEIDENHAIN GmbH, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted. A "Related Proceedings Appendix" is nevertheless attached hereto and appears on the one (1) page numbered "Related Proceedings Appendix."

11. CONCLUSION

For at least the reasons indicated above, Appellant respectfully submits that the art of record does not disclose or suggest the subject matter as recited in the claims of the above-identified application. Accordingly, it is respectfully submitted that the subject matter as set forth in the claims of the present application is patentable.

In view of all of the foregoing, reversal of the rejections set forth in the Final Office Action is therefore respectfully requested.

Respectfully submitted,

Dated: April 29, 2009

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CLAIMS APPENDIX

21. A method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale, comprising:

converting each of the analog signals into a digital data stream by a sigma-delta modulator;

generating a string of results by combining the data streams with correctional values and subsequently combining the data streams with one another;

generating from the string of results (a) new correctional values in accordance with a quality criterion that is to be satisfied during interpolation and (b) output signals of the interpolation;

accumulating over a specifiable time interval values of the string of results for generating the correctional values and the output signals; and

using a signal sequence generated by the accumulation as an address sequence for generating the correctional values and for generating the output signal.

22. The method according to claim 21, wherein the values of the string of results are accumulated in the accumulating step in a filter.

23. The method according to claim 22, wherein the filter includes an integrator.

24. The method according to claim 21, further comprising forming the address sequence by the accumulation, the address sequence including address values that represent phase information of the analog signals.

25. The method according to claim 24, wherein the output signals are generated in the output signal generating step from the address sequence by low-pass filtering and assignment of the address values.

26. The method according to claim 24, wherein the address values are a linear function of the phase of the periodic analog signals when the quality criterion is satisfied.

27. The method according to claim 21, where address values of the address sequence represent a phase value having a fractional proportion.

28. The method according to claim 27, wherein the correctional values are generated in the correctional value generating step in accordance with a high-value part of the address sequence, the high-value part corresponding to an integer proportion of the address values.

29. The method according to claim 27, wherein the output signals are generated in the output signal generating step in accordance with a most-significant part and a least-significant part of the address sequence, the least-significant part corresponding to a fractional proportion of the address values, the most-significant part corresponding to an integer proportion of the address values.

30. The method according to claim 21, wherein the output signals are generated recursively in the output signal generating step by generating new correctional values in accordance with the quality criterion and combining the new correctional values with the data streams until the quality criterion is satisfied.

31. The method according to claim 21, further comprising storing possible correction values as predefined values in an assignment unit.

32. The method according to claim 31, further comprising selecting the correction values to be combined with the data of the data streams in accordance with the quality criterion as a function of address values of the address sequence.

33. The method according to claim 21, wherein the correctional values correspond to values of a trigonometric function.

34. The method according to claim 21, wherein the analog signals are phase-shifted by 90° with respect to each other.

35. The method according to claim 21, wherein the analog signals are substantially sinusoidal.

36. The method according to claim 21, wherein the combining step includes multiplicatively combining individual data of the digital data streams with a respective correctional value and subsequently combining data of different data streams with one another by one of (a) addition and (b) subtraction.

37. The method according to claim 21, wherein individual data of the digital data streams each have a word width of one bit.

38. The method according to claim 36, wherein the combining step includes reducing the combination of two data of the digital data streams with the correctional values and with each other to one of (a) an additive and (b) a subtractive combination of two correctional values.

39. The method according to claim 38, wherein the combining step includes combining the combination to one of four possibilities of the combination of the correctional values by one of (a) addition and (b) subtraction.

40. A device for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to each other and which are generated by scanning a measuring scale, comprising:

a sigma-delta modulator configured to convert the analog signals to a respective digital data stream;

an arithmetic unit configured to generate a string of results in accordance with a combination of the data streams with correctional values and in accordance with subsequent combination of the data streams with one another;

an arrangement configured to generate, from the string of results, (a) new correctional values in accordance with a quality criterion that is to be satisfied during the interpolation and (b) output signals of the interpolation;

a filter configured to accumulate values of the string of results over a specified time interval to generate an address sequence to control the arithmetic unit to guide the string of results to satisfy the quality criterion; and

an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation.

41. A method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale, comprising:

converting each of the analog signals into a digital data stream by a sigma-delta modulator;

generating a string of results by combining the data streams with correctional values and subsequently combining the data streams with one another;

generating from the string of results a combination output in accordance with a quality criterion that is to be satisfied during interpolation;

accumulating over a specifiable time interval values of the combination output for generating the correctional values and output signals; and

using a signal sequence generated by the accumulation as an address sequence for generating the correctional values and for generating the output signal.

42. A device for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to each other and which are generated by scanning a measuring scale, comprising:

a sigma-delta modulator configured to convert the analog signals to a respective digital data stream;

an arithmetic unit configured to generate a string of results in accordance with a combination of the data streams with correctional values and subsequent combination of the data streams with one another;

an arrangement configured to generate, from the string of results a combination output in accordance with a quality criterion that is to be satisfied during the interpolation;

a filter configured to accumulate values of the combination output over a specified time interval to generate an address sequence to control the arithmetic unit to guide the string of results to satisfy the quality criterion; and

an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation.

EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellant in the appeal.

RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2 of this Appeal Brief, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellant or the assignee, DR. JOHANNES HEIDENHAIN GmbH, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted.